Claims

[c1] In an integrated circuit chip having a programmable reference data table for holding information used to control at least one circuit block in said chip, a method of improving the performance of said chip comprising
(A) testing said chip to determine data comprising operating voltages at different clock speeds; and
(B) entering values based on said data into said reference data table.

[c2] A method according to Claim 1 wherein said values are permanently entered into said reference data table.

[c3] A method according to Claim 2 wherein said values are entered using an anti-fuse method.

[c4] A method according to Claim 2 wherein said values are entered using a non-volatile memory method.

[c5] A method according to Claim 1 wherein said values are tentatively entered into said reference data table.

[c6] A method according to Claim 1 wherein said chip is for use in a battery-powered computer and is tested at 2 to 4 different supply voltages between 1 and 4 volts, 2 to 4 different back-bias voltages between -0.5 and +0.5 volts, and 2 to 4 different clock speeds between 1 and 300 MHz.

[c7] A method according to Claim 1 wherein said chip is for use in a plug-in computer and is tested at 2 to 4 different supply voltages between 1 and 4 volts, 2 to 4 different back-bias voltages between -.05 and +0.5 volts, and 2 to 4 different clock speeds between 0.2 and 2 GHz.

[c8] A method according to Claim 1 wherein said chip has only a single circuit block.

[c9] A method according to Claim 1 wherein said chip has numerous circuit blocks.

[c10] A method according to Claim 1 wherein said chip is tested when it is on a wafer.

[c11] A method according to Claim 1 wherein said chip is tested after it has been cut

from a wafer.

[c12] A method according to Claim 1 wherein said data comprises at least one supply voltage, at least one back-bias voltage, and at least one clock rate.

[c13] A method according to Claim 1 wherein said data comprises the minimum supply voltages and minimum back bias voltages at which the chip successfully executed a program at different clock speeds.

[c14] A method according to Claim 1 wherein said data comprises at least one supply voltage, at least one back-bias voltage, at least one clock rate, at least one data bus width, or at least one power latency value.

[c15] A method according to Claim 1 wherein the performance that is improved is the operating clock speed.

[c16] A method according to Claim 1 wherein the performance that is improved is the operating voltage range.

[c17] A microprocessor chip made according to the method of Claim 1.

[c18] An integrated circuit chip made according to the method of Claim 1.

[c19] A computer comprising an integrated circuit chip according to Claim 18.

[c20] A computer according to Claim 19 that is battery powered.

[c21] In a wafer having a multiplicity of integrated circuit chips thereon, each having a programmable reference data table for holding data including the supply voltage, back-bias voltage, and clock speed to be used to control at least one circuit block on said integrated circuit chip, a method of programming the reference data table of a chip with improved values comprising
(A) testing the chip to determine data comprising at least a minimum supply voltage and a minimum back-bias voltage at which said chip can operate at at least one clock speed; and
(B) based on said data, entering values into the chip's programmable reference data table comprising a supply voltage and back-bias voltage to be used to attain said at least one clock speed.

[c22] An integrated circuit chip made according to the method of Claim 21.

[c23] A computer comprising an integrated circuit chip according to Claim 22.

[c24] In a wafer having a multiplicity of integrated circuit chips thereon, each of said chips having a programmable reference data table for holding, for at least one circuit block in said chip, values comprising supply voltages and back-bias voltages to be used to attain at least two different clock speeds, a method of improving the power usage requirements of said chip comprising

(A) executing at least one program on said chip at at least two different supply voltages, at least two different back-bias voltages, and at least two different clock speeds;

(B) collecting data comprising the lowest supply voltage and the lowest back-bias voltage at which said chip successfully executed said program at each clock speed tested;

(C) based on said data, determining values comprising the optimal supply voltages and back bias voltages to be used for at least two different clock speeds; and

(D) entering said values into said table.

[c25] A wafer having at least one chip thereon programmed according to the method of Claim 24.